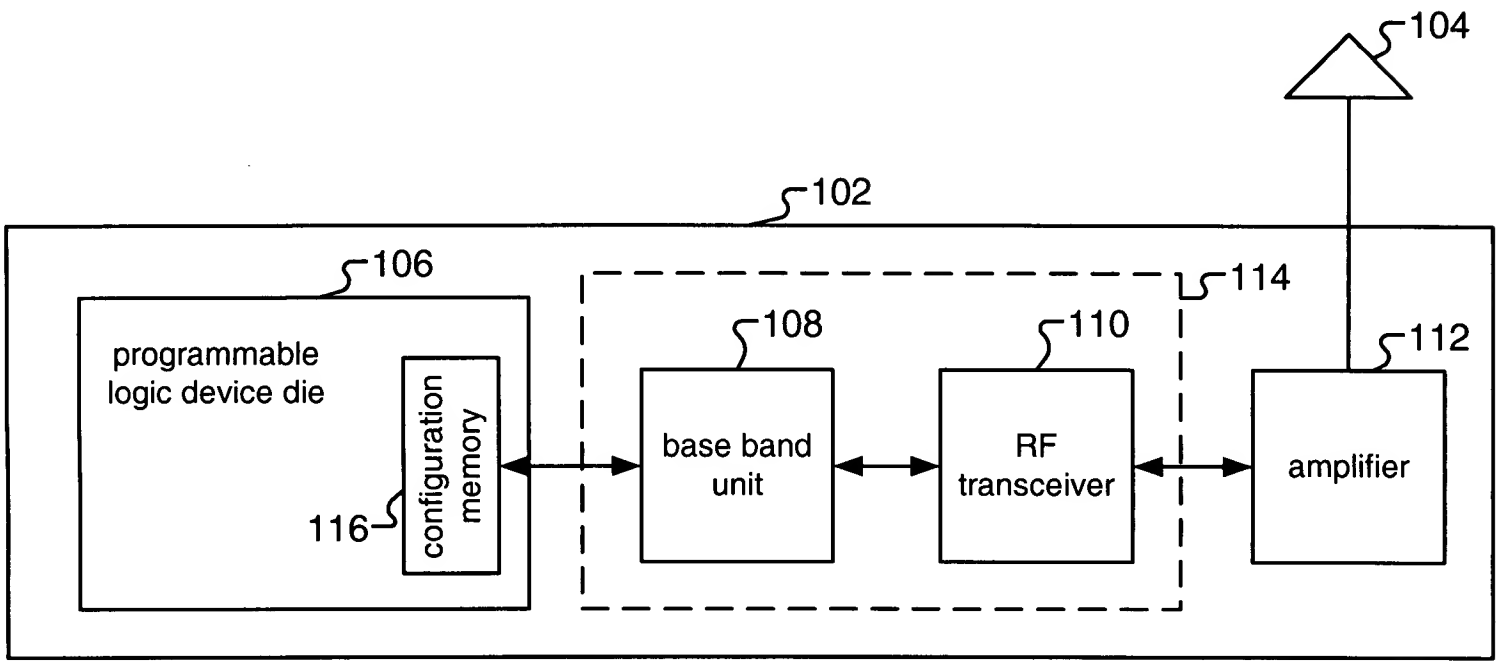
104
102
106
programmable
logic device die
configuration
memory
116
114
108
base band
unit
110
RF
transceiver
112
amplifier

FIG. 1

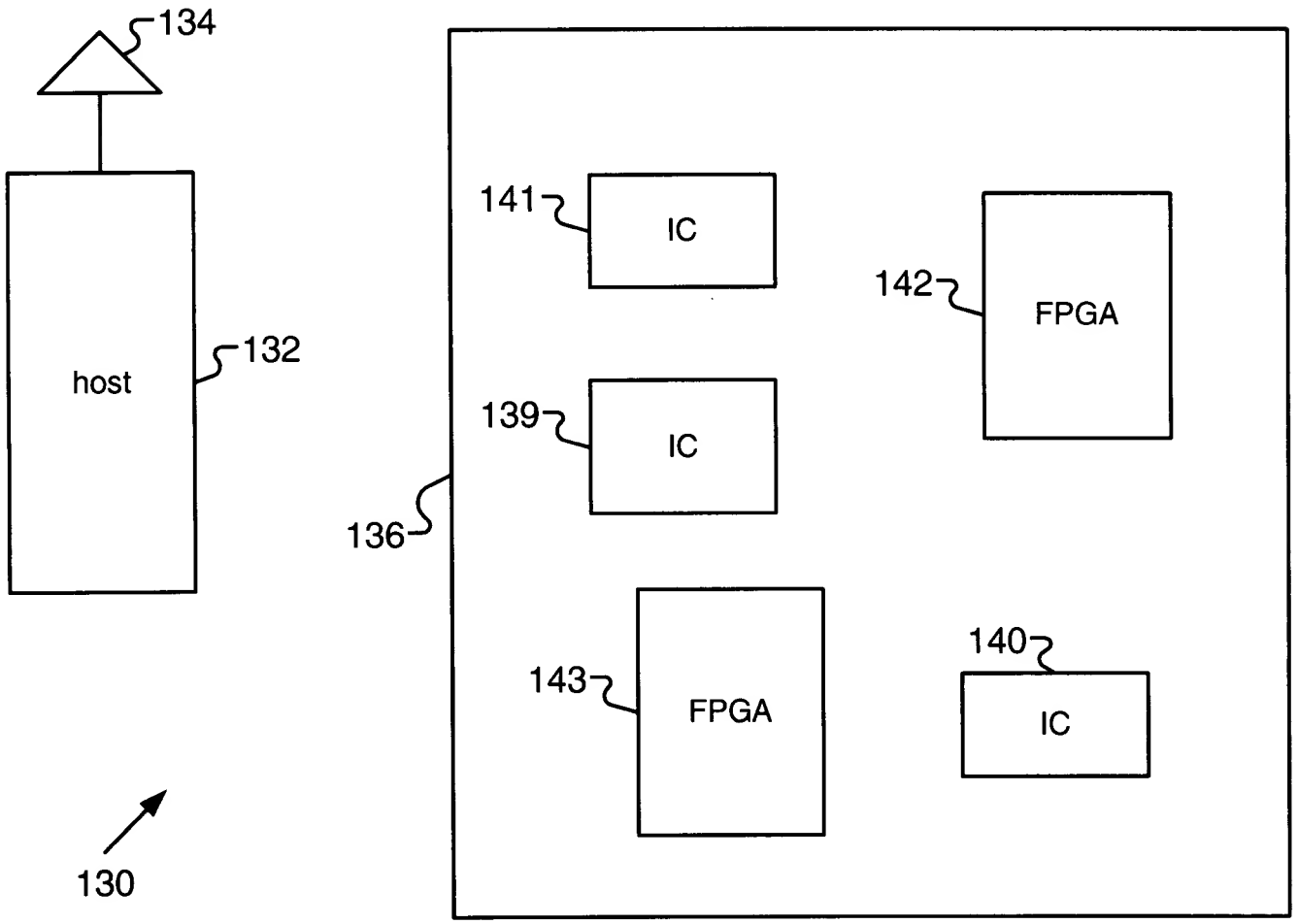

FIG. 2

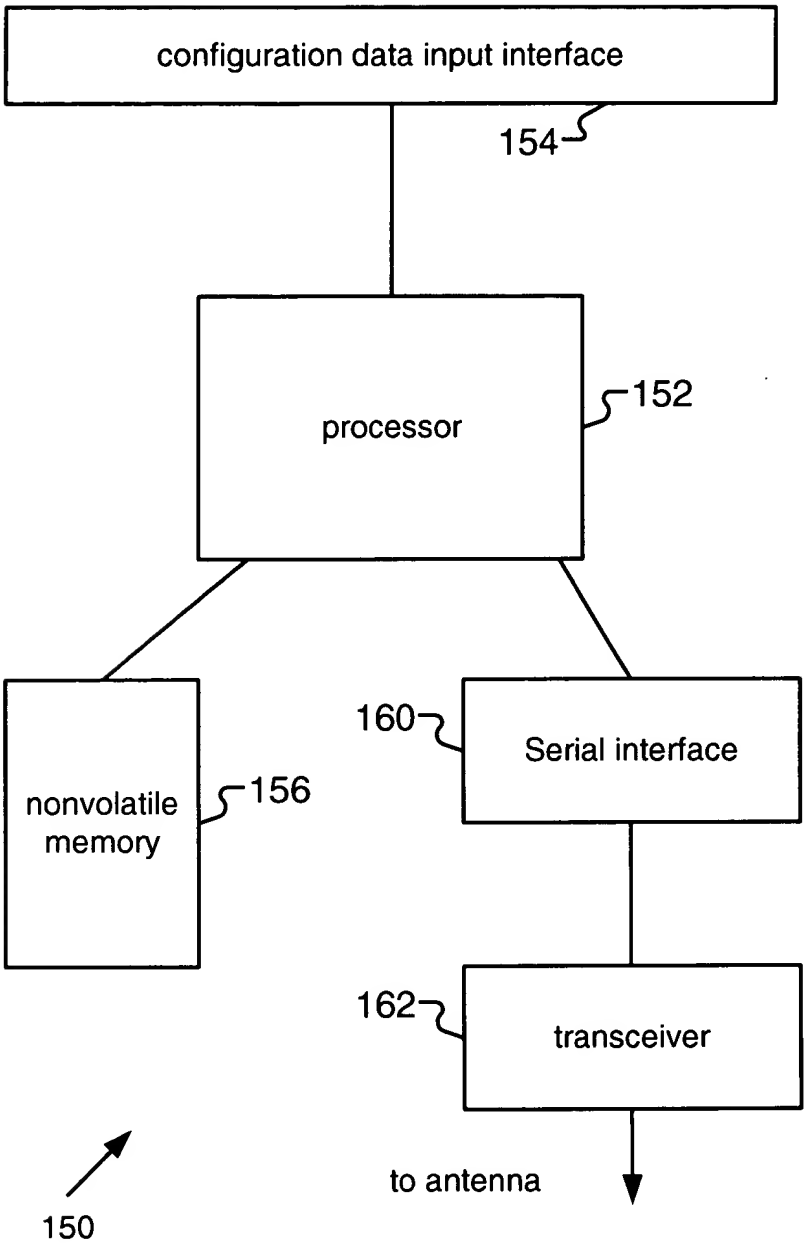
configuration data input interface
154
processor
152
nonvolatile memory
156
160
Serial interface
162
transceiver
to antenna
150

FIG. 3

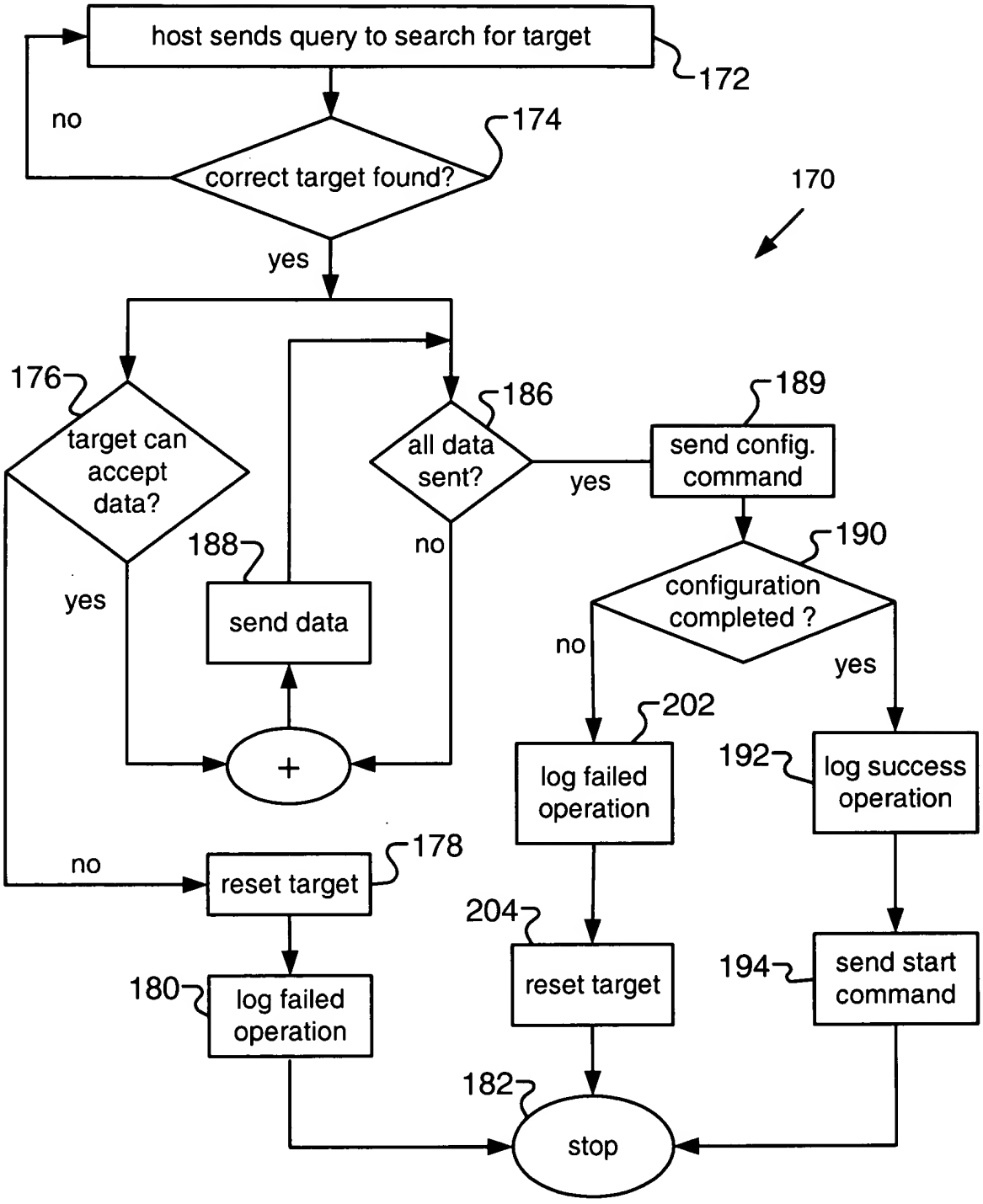
host sends query to search for target
172
no
174
correct target found?
170
yes
176
target can accept data?
186
all data sent?
189
send config. command
yes
188
send data
no
190
configuration completed ?
yes
no
202
log failed operation
192
log success operation
+
no
178
reset target
204
reset target
194
send start command
180
log failed operation
182
stop

FIG. 4

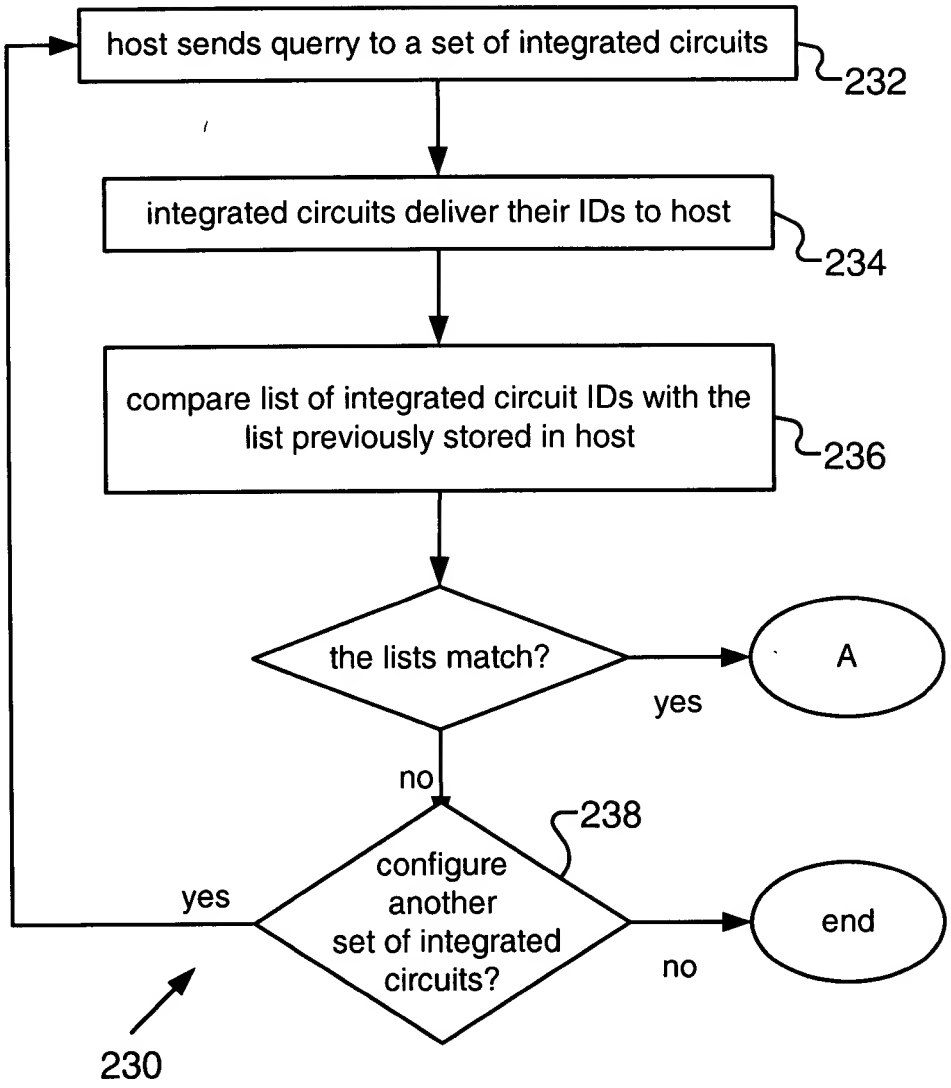
host sends querry to a set of integrated circuits
232
integrated circuits deliver their IDs to host
234
compare list of integrated circuit IDs with the list previously stored in host
236
the lists match?
yes
A
no
238
configure another set of integrated circuits?
yes
no
end
230

FIG. 5A

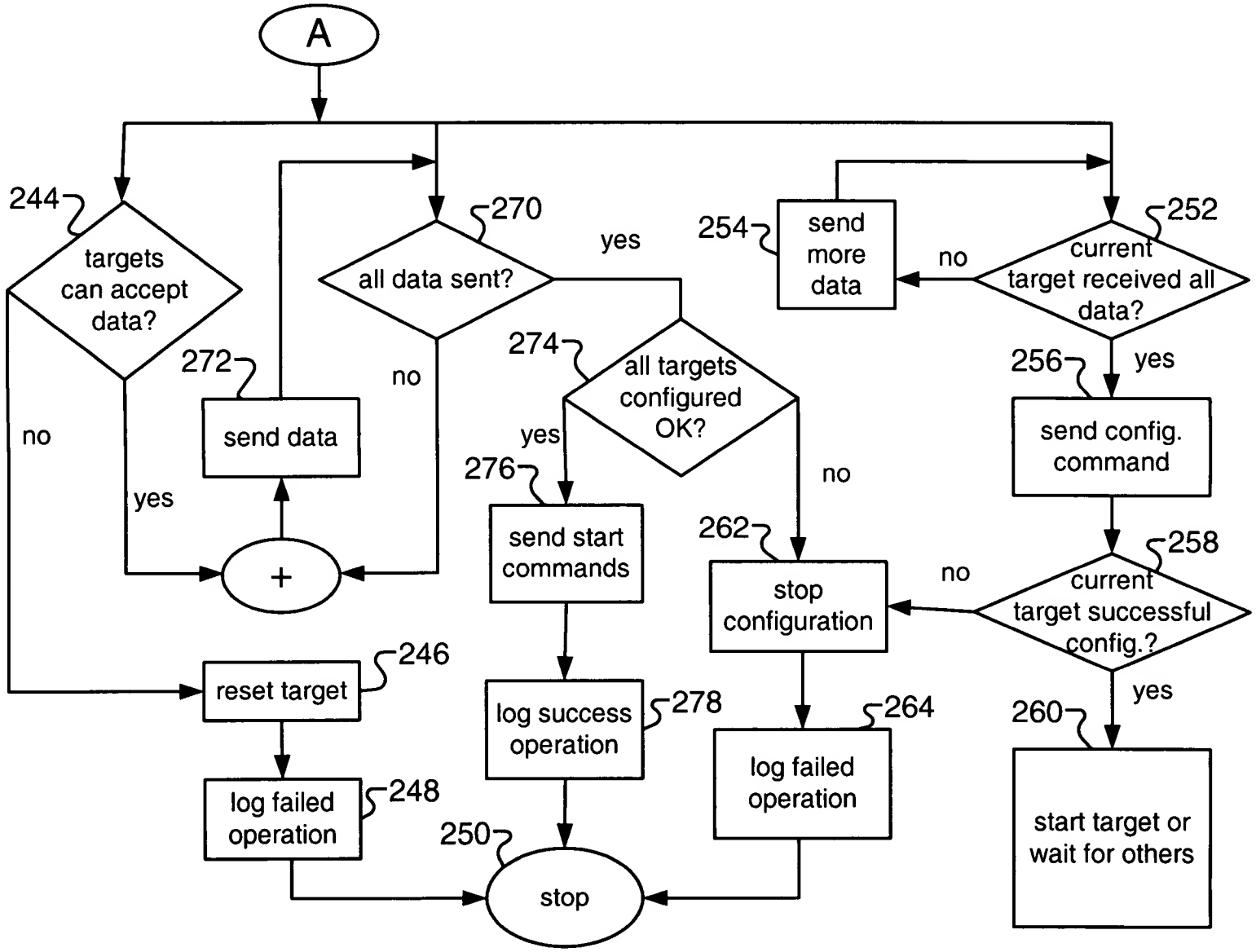
A
244
targets can accept data?
no
yes
272
send data
+
270
all data sent?
yes
no
274
all targets configured OK?
yes
no
276
send start commands
262
stop configuration
254
send more data
no
252
current target received all data?
yes
256
send config. command
258
current target successful config.?
no
yes
260
start target or wait for others
246
reset target
248
log failed operation
278
log success operation
264
log failed operation
250
stop

FIG. 5B

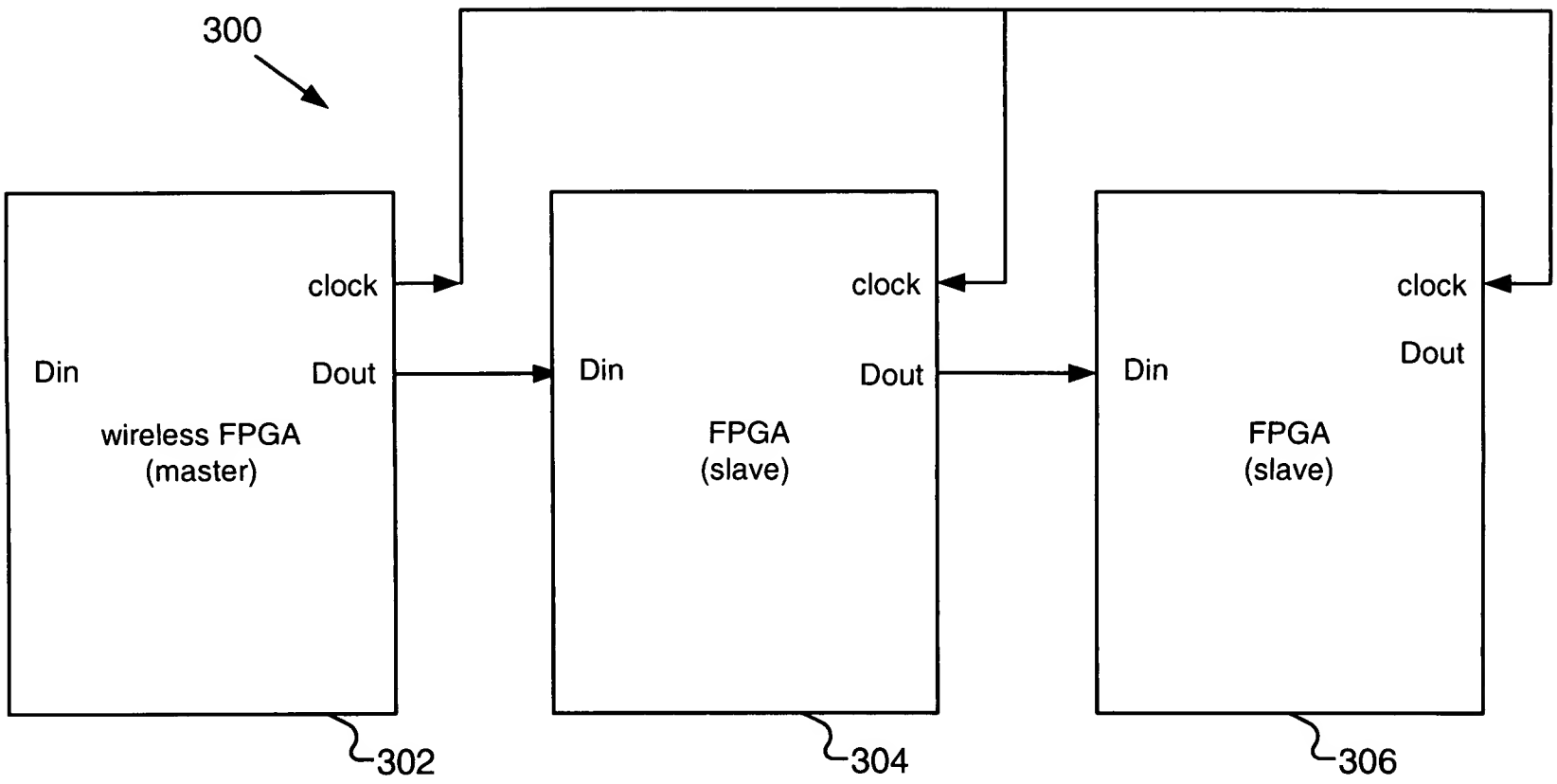
300
clock
Din
Dout
wireless FPGA
(master)
302
clock
Din
Dout
FPGA
(slave)
304
clock
Dout
Din
FPGA
(slave)
306

FIG. 6